Docket No.: 50090-234

UTILITY PATENT APPLICATION UNDER 37 CFR 1.53(b)

Box PATENT APPLICATION
Assistant Commissioner for Patents
Washington, DC 20231
Sir:

Transmitted herewith for filing is the patent application of:

INVENTOR: Kozo HARADA, Hiroshi SAWANO
FOR: SEMICONDUCTOR DEVICE HAVING DENSELY STACKED SEMICONDUCTOR CHIPS

Enclosed are:

- ☒ 24 pages of specification, claims, abstract.
- ☒ Declaration and Power of Attorney.
- ☒ Priority Claimed.
- ☒ Certified copy of Japanese Patent Application No. 2000-033790
- ☒ 6 sheets of formal drawing.
- ☒ An assignment of the invention to Mitsubishi Denki Kabushiki Kaisha and the assignment recordation fee.
- ☐ An associate power of attorney.
- ☐ A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27.
- ☒ Information Disclosure Statement, Form PTO-1449 and reference.
- ☒ Return Receipt Postcard
- ☐

The filing fee has been calculated as shown below:

	NO. OF CLAIMS		EXTRA CLAIMS	RATE	AMOUNT
Total Claims	16	-20	0	$18.00	$0.00
Independent Claims	4	-3	1	$78.00	$78.00
				Multiple Dependent Claim(s)	$0.00
				Basic Fee	$690.00
				Total of Above Calculations	$768.00
				Less ½ for Small Entity	$0.00
				Assignment & Recording Fee	$40.00
				Total Fee	$808.00

☒ Please charge my Deposit Account No. 500417 in the amount of $808.00. A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 500417. A duplicate copy is enclosed.

- ☒ Any additional filing fees required under 37 CFR 1.16.

☒ The Commissioner is hereby authorized to charge payment of the following fees during the pendency of this application or credit any overpayment to Deposit Account No. 500417. A duplicate copy of this sheet is enclosed.

- ☒ Any patent application processing fees under 37 CFR 1.17.
- ☒ Any filing fees under 37 CFR 1.16 for presentation of extra claims.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Arthur J. Steiner
Registration No. 26,106

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 AJS:klm
Date: August 11, 2000
Facsimile: (202) 756-8087

SEMICONDUCTOR DEVICE HAVING DENSELY STACKED SEMICONDUCTOR CHIPS

Background of the Invention

Field of the Invention

The present invention relates to a semiconductor device having densely packaged semiconductor chips, in particular of the same size.

Background Art

Fig. 21 is a sectional view showing a structure of a conventional semiconductor device having stacked semiconductor chips.

A conventional method for the high-density packaging of semiconductor chips will be described below. First, on a substrate 10q provided with conductive layers 10p, the largest chip 1p among semiconductor chips to be packaged is die-bonded with on-the-chip electrodes facing up. Similarly, a semiconductor chip 1q smaller than the semiconductor chip 1p previously bonded is die-bonded on the semiconductor chip 1p. However, the semiconductor chip to be die-bonded on the underlying semiconductor chip must always be die-bonded on the space where there are no electrodes of the underlying semiconductor chip. Next, the electrodes of each of thus stacked semiconductor chips 1p and 1q are electrically connected to conductive layers 10p on the substrate 10q using wire bonding.

However, when semiconductor chips of the same size are densely mounted by a conventional method, the electrodes of an underlying semiconductor chip are always hidden by the die-bonded overlying semiconductor chip, and cannot be electrically connected to conductive layers on the substrate.

Summary of the Invention

Therefore, the object of the present invention is to solve such problems of conventional methods, and to provide a semiconductor device which enables the high-density packaging of semiconductor chips even of the same size.

According to one aspect of the present invention, a semiconductor device or a semiconductor device unit comprises a semiconductor chip, at least a first electrode formed on the first major surface of the semiconductor chip, and at least a second electrode or an insulation layer formed on the second major surface opposite to the first major surface. Further; at least a conductive member is provided for connecting the first electrode with the second electrode or the insulation layer, and the conductive member is formed along the outer circumference of at least a side of the semiconductor chip.

According to another aspect of the present invention, a semiconductor device comprises a plurality of the semiconductor device units which are stacked each other, and the conductive members are connected to each other.

According to another aspect of the present invention, a semiconductor device comprises a plurality of the semiconductor device units and a packaging board for mounting the plurality of semiconductor device units. The semiconductor device units are placed on the packaging board so as to have a predetermined angle to the packaging board, and the conductive members of the semiconductor device units are connected to the packaging board.

According to another aspect of the present invention, a semiconductor device comprises a plurality of semiconductor chips each having electrodes formed on the major surface thereof, and a plurality of spacer members each having conductive pattern on the surface thereof.

The semiconductor chips and the spacer members are stacked alternately such that the electrodes of the semiconductor chips are electrically connected to the conductive patterns of the spacer members,

and the conductive patterns of the spacer members are electrically connected to each other.

Other features and advantages of the invention will be apparent from the following description taken in connection with the accompanying drawings.

Brief Description of the Drawings

Fig. 1 is a sectional view showing a structure of a semiconductor device according to a First Embodiment of the present invention.

Figs. 2 and 3 are sectional views showing structures of semiconductor devices according to a Second Embodiment of the present invention.

Figs. 4 and 5 are sectional views showing structures of semiconductor devices according to a Third Embodiment of the present invention.

Figs. 6 and 7 are sectional views showing structures of semiconductor devices according to a Fourth Embodiment of the present invention.

Figs. 8 through 10 are sectional views showing structures of semiconductor devices according to a Fifth Embodiment of the present invention.

Figs. 11 through 13 are sectional views showing structures of semiconductor devices according to a Sixth Embodiment of the present invention.

Fig. 14 is a sectional view showing a structure of a semiconductor device according to a Seventh Embodiment of the present invention.

Fig. 15 is a sectional view showing a structure of a semiconductor device according to an Eighth Embodiment of the present invention.

Fig. 16 is a sectional view showing a structure of a semiconductor device according to a Ninth Embodiment of the present invention.

Figs. 17 and 18 are sectional views showing the structure of a semiconductor device according to a Tenth Embodiment of the present invention.

Figs. 19 and 20 are sectional views showing a structure of a semiconductor device according to an Eleventh Embodiment of the present invention.

Fig. 21 is a sectional view showing a structure of a conventional semiconductor device having stacked semiconductor chips.

Detailed Description of the Preferred Embodiments

The embodiments of the present invention will be described below referring to the drawings. In the drawings, the same or like elements are indicated by the same symbols, and the description thereof is simplified or omitted.

First Embodiment

Fig. 1 is a sectional view showing a structure of a semiconductor device according to a First Embodiment.

In Fig. 1, reference numeral 1 indicates a semiconductor chip, 2 indicates a top-surface electrode (first electrode) formed on the top surface (first major surface) of the semiconductor chip 1, 3 indicates a back-surface electrode (second electrode) formed on the back surface (second major surface) of the semiconductor chip 1, and 4 indicates a conductive wire (conductor member) connecting the top-surface electrode 2 with the back-surface electrode 3.

The semiconductor device of this embodiment comprises a semiconductor chip 1 having electrodes 2 and 3 on the top and back surfaces, respectively, in which the top-surface electrode 2 is electrically connected with the back-surface electrode 3 by wire bonding.

This semiconductor device is produced by bonding an end of the conductive wire 4 to the top-surface electrode 2, inverting the

semiconductor chip 1 upside down, and bonding the other end of the conductive wire 4 to the back-surface electrode 3.

In the semiconductor device according to this embodiment, as Fig. 1 shows, first electrodes are formed on the top surface (first major surface) of a semiconductor chip, second electrodes are formed on the back surface (second major surface) opposite to the first major surface, and conductive members for connecting the first electrodes with the second electrodes are formed along the outer circumference of the sides of the semiconductor chip.

In other words, as Fig. 1 shows, in a semiconductor chip having electrodes formed on top and back surfaces, the top-surface electrodes are loop-connected with the back-surface electrodes by wire bonding.

The semiconductor device having such a structure enables high-density packaging by stacking even if the semiconductor chips have the same size.

Second Embodiment

Figs. 2 and 3 are sectional views showing structures of semiconductor devices according to a Second Embodiment.

In Figs. 2 and 3, reference numeral 5 indicates a conductive clip having elasticity for clamping objects, 6 indicates an insulation layer provided by a surface insulation treatment, and 7 indicates a semiconductor chip having the insulation layer 6.

One of the semiconductor device of this embodiment comprises a semiconductor chip 1 having electrodes 2 and 3 on the top and back surfaces, respectively, and is provided with conductive clips 5 such that an end thereof contacts with the top-surface electrodes 2 and the other end contacts with the back-surface electrodes 3, and the connection of top- and back-surface electrodes 2 and 3 is retained by the elasticity thereof as Fig. 2 shows.

Alternatively, as Fig. 3 shows, another one of the semiconductor device of this embodiment comprises a semiconductor chip 7 having top-surface electrodes 2 and an insulation layer 6 insulation-treated and formed on the back surface, respectively, and is provided with conductive clips 5 such that an end thereof contacts with the top-surface electrodes 2 and the other end contacts with the insulation layer 6, and the holding is retained by the elasticity thereof.

In other words, one of the semiconductor devices according to this embodiment comprises a semiconductor chip 1 provided with electrodes 2 and 3 on the top and back surfaces, respectively, in which the top-surface electrode 2 is electrically connected with the back-surface electrode 3 by a conductive clip 5 as Fig. 2 shows. Alternatively, as Fig. 3 shows, another one of the semiconductor devices of this embodiment comprises a semiconductor chip 7 having electrodes 2 provided on the top surface and an insulation layer 6 insulation-treated and provided on the back surface, in which the top-surface electrode 2 and the insulation layer 6 on the back surface are clipped together by a conductive clip 5.

The semiconductor device having such a structure enables high-density packaging by stacking even if the semiconductor chips have the same size.

Third Embodiment

Figs. 4 and 5 are sectional views showing structures of semiconductor devices according to a Third Embodiment.

In Figs. 4 and 5, reference numeral 8 indicates a conductive material injection-molded over the surfaces of the semiconductor chip 1.

One of the semiconductor device according to this embodiment comprises a semiconductor chip 1 provided with electrodes 2 and 3 on the top and back surfaces, respectively, in which a conductive material

8 is injection-molded over the area from the top-surface electrodes 2 to the back-surface electrodes 3, as Fig. 4 shows.

Alternatively, as Fig. 5 shows, the other of the semiconductor device of this embodiment comprises a semiconductor chip 7 having electrodes 2 provided on the top surface and an insulation layer 6 provided on the back surface, in which a conductive material 8 is formed by injection molding or the like method over the area from the top-surface electrodes 2 to the insulation layer 6.

In other words, one of the semiconductor devices according to this embodiment comprises a semiconductor chip 1 provided with electrodes 2 and 3 on the top and back surfaces, respectively, in which the top-surface electrode 2 is electrically connected with the back-surface electrode 3 by injection-molding a conductive material as Fig. 4 shows. Alternatively, as Fig. 5 shows, the other of the semiconductor devices of this embodiment comprises a semiconductor chip 7 having electrodes 2 provided on the top surface and an insulation layer 6 insulation-treated and provided on the back surface, in which the top-surface electrode 2 and the insulation layer on the back surface are covered by injection-molded conductive material.

The semiconductor device having such a structure enables high-density packaging by stacking even if the semiconductor chips have the same size.

Fourth Embodiment

Figs. 6 and 7 are sectional views showing structures of semiconductor devices according to a Fourth Embodiment.

In Figs. 6 and 7, reference numeral 1 indicates one of stacked semiconductor chips, reference numeral 1′ indicates the other of stacked semiconductor chips, reference numeral 4 indicates one of conductive members, and reference numeral 4′ indicates the other of conductive members. In Fig. 7, reference numeral 2a indicates a first

wiring pattern drawn from the top-surface electrode (first electrode) 2, reference numeral 3a indicates a second wiring pattern drawn from the back-surface electrode (second electrode) 3, and reference numeral 23 indicates a bump. A unit comprising a semiconductor chip 1, surface electrodes 2, 3 or an insulation layer 6, and conductive member 4 is named as a semiconductor device unit in this embodiment.

One of the semiconductor devices of this embodiment is constituted, as Fig. 6 shows, by stacking at least two semiconductor chips or semiconductor device units described referring to Fig. 1, and by contacting the conductive wires 4, which is connected to the top-surface electrodes 2 of the underlying semiconductor chip 1, with the conductive wires 4', which is connected to the back-surface electrodes 3 of the overlying semiconductor chip 1'. The conductive wires 4 and 4' may be joined by solder or the like.

Alternatively, as Fig. 7 shows, the semiconductor device of this embodiment is constituted, by stacking at least two semiconductor chips or semiconductor device units described referring to Fig. 1, and connecting the wiring pattern 2a, which extends from the top-surface electrodes 2 of the underlying semiconductor chip 1, to the wiring pattern 3a, which extends from the back-surface electrodes 3 of the overlying semiconductor chip 1', by means of a bump 23.

In other words, one of the stacked semiconductor devices according to this embodiment comprises, as Fig. 6 shows, a plurality of stacked semiconductor chips 1, 1', wherein a semiconductor chips 1' is stacked on a semiconductor chip 1'. Each of the semiconductor chips 1, 1' has top-surface electrodes (first electrodes) 2 on the top surface (first major surface), and back-surface electrodes (second electrodes) 3 on the back surface (second major surface) opposite to the top surface (first major surface). Each of the semiconductor chips 1, 1' has the conductive members 4, 4' for connecting the top-surface electrodes 2 with the back-surface electrodes 3 along the outer circumstance of the

sides of the semiconductor chips 1, 1' respectively. The upper semiconductor chip 1' is so positioned on the lower semiconductor chip 1 that the back-surface electrodes 3 of the upper semiconductor chip 1' faces the top-surface electrodes 2 of the lower semiconductor chip 1. The conductive members 4, 4' of the semiconductor chips 1, 1' adjacent to each other are electrically and mechanically connected.

Another stacked semiconductor device according to this embodiment comprises, as Fig. 7 shows, a lower semiconductor chip 1 having a first wiring pattern 2a drawn from the top-surface electrodes (first electrodes) 2, and a upper semiconductor chip 1' having a second wiring pattern 3a drawn from the back-surface electrodes (second electrodes) 3, and a bump 23 is provided between the first wiring pattern 2a and the second wiring pattern 3a for electrically connecting the both wiring patterns.

Still in other words, one of the stacked semiconductor device of this embodiment comprises, as Fig. 6 shows, semiconductor chips 1, 1' in the stacked structure. Each of the semiconductor chips 1, 1' has electrodes 2, 3 on top and back surfaces, respectively, and the top-surface electrodes 2 are loop-connected with back-surface electrodes 3 by wire bonding of the conductive wires 4, 4' respectively. The mutual electrical connection is performed by connecting the conductive materials (wires) 4 and 4'. The other of the stacked semiconductor device of this embodiment comprises, as Fig. 7 shows, the stacked semiconductor chips 1, 1', in which the mutual electrical connection is performed by the conductive wires 4 and 4', and by the metal bump 23 formed between the wiring patterns 2a and 3a drawn from the electrodes 2 and 3 of the lower and upper semiconductor chips respectively.

In this way, a stacked semiconductor device can be produced by stacking semiconductor chips or semiconductor device units of the same size, and electrically connecting upper and lower semiconductor chips.

Fifth Embodiment

Figs. 8 through 10 are sectional views showing structures of semiconductor devices according to a Fifth Embodiment.

In Figs. 8 through 10, reference numeral 5 indicates a conductive clip, 5′ indicates another conductive clip, 7 indicates one of stacked semiconductor chips, and 7′ indicates the other of stacked semiconductor chips. A unit comprising a semiconductor chip 1, surface electrodes 2, 3 or an insulation layer 6, and clip 5 is named as a semiconductor device unit in this embodiment.

The semiconductor device of this embodiment is constituted, as Fig. 8 shows, by stacking at least two semiconductor chips 1, 1′ or semiconductor device units described referring to Fig. 2, and by contacting the conductive clip 5, which is provided on the underlying semiconductor chip 1, with the conductive clip 5′, which is provided on the overlying semiconductor chip 1′. The conductive clips 5 and 5′ may be metal joined by solder or the like.

As another example, as Fig. 9 shows, the semiconductor device of this embodiment is constituted by stacking at least two semiconductor chips or semiconductor device units described referring to Fig. 3, and by contacting the conductive clip 5 provided on the underlying semiconductor chip 7 to the conductive clip 5′ provided on the overlying semiconductor chip 7′. The conductive clips 5 and 5′ may be metal joined by solder or the like.

As a further example, as Fig. 10 shows, the semiconductor device of this embodiment is constituted by stacking at least two semiconductor chips or semiconductor device units described referring to Fig. 2, and by connecting the first wiring pattern 2a, extending from the top-surface electrode 2 of the underlying semiconductor chip 1, with the second wiring pattern 3a extending from the back-surface electrode 3 of the overlying semiconductor chip 1′ using a bump 23.

In other words, the stacked semiconductor device of this embodiment, as Figs. 8 through 10 show, comprises at least two stacked semiconductor chips each having electrodes 2 formed on the top surface and electrodes 3 or insulation layers 6 formed on the back surface. Each of the top-surface electrodes 2 is connected with the back-surface electrode 3 or insulation layers 6 using conductive clips 5 or 5'. Mutual electrical connection is performed by connecting the conductive clips 5 and 5' to each other, or by using the conductive clips 5 and 5' and a metal bump 23 formed on the wiring patterns 2a and 3a drawn from electrodes 2 and 3 of the lower and upper semiconductor chips, respectively.

In this way, a stacked semiconductor device can be produced by stacking semiconductor chips of the same size, and electrically connecting upper and lower semiconductor chips.

Sixth Embodiment

Figs. 11 through 13 are sectional views showing structures of semiconductor devices according to a Sixth Embodiment.

In Figs. 11 through 13, reference numeral 8 indicates a conductive material or conductive layer, and 8' indicates another conductive material or conductive layer. A unit comprising a semiconductor chip 1, surface electrodes 2, 3 or an insulation layer 6, and conductive material 8 is named as a semiconductor device unit in this embodiment.

The semiconductor device of this embodiment is constituted, as Fig. 11 shows, by stacking at least two semiconductor chips or semiconductor device units described referring to Fig. 4, and connecting injection-molded conductive materials 8 on the underlying semiconductor chip 1 with injection-molded conductive materials 8' on the overlying semiconductor chip 1'.

As another example, as Fig. 12 shows, the semiconductor device of this embodiment is constituted by stacking at least two semiconductor

chips or semiconductor device units described referring to Fig. 5, and connecting injection-molded conductive materials 8 on the underlying semiconductor chip 7 with injection-molded conductive materials 8′ on the overlying semiconductor chip 7′.

As a further example, as Fig. 13 shows, the semiconductor device of this embodiment is constituted by stacking at least two semiconductor chips or semiconductor device units described referring to Fig. 4, and connecting the first wiring pattern 2a extending from the top-surface electrode 2 of the underlying semiconductor chip 1 with the second wiring pattern 3a extending from the back-surface electrode 3 of the overlying semiconductor chip 1′ using a bump 23.

In other words, the stacked semiconductor device of this embodiment, as Figs. 11 through 13 show, comprises at least two semiconductor chips each having electrodes 2 and 3 formed on the top and back surfaces, respectively. Each of the top-surface electrodes 2 are connected with the back-surface electrodes 3 by injection-molded conductive materials 8 and 8′. Alternatively, the back surface is insulation-treated, and the top-surface electrodes 2 are connected with the insulation layers 6 on the back-surfaces by injection-molded conductive materials 8 and 8′. The mutual electrical connection is performed by connecting the conductive materials 8 and 8′ to each other, or by using the conductive materials 8 and 8′, and a metal bump 23 formed on the wiring patterns 2a and 3a drawn from electrodes 2 and 3 of the lower and upper semiconductor chips 1, 1′, respectively.

In this way, a stacked semiconductor device can be produced by stacking semiconductor chips of the same size, and electrically connecting upper and lower semiconductor chips.

Seventh Embodiment

Fig. 14 is a sectional view showing a structure of a semiconductor device according to a Seventh Embodiment.

In Fig. 14, reference numeral 9 indicates conductive patterns, and 10 indicates a packaging board. A unit comprising a semiconductor chip 1, surface electrodes 2 and 3, and conductive member 4 is named as a semiconductor device unit in this embodiment.

The semiconductor device of the present invention is constituted by providing conductive wires 4 which electrically connect the top-surface electrodes 2 with the back-surface electrodes 3 in the semiconductor device unit described referring to Fig. 1 on the one end of each of the semiconductor chips 1, placing the semiconductor chips 1 perpendicularly to the packaging board 10 having conductive patterns 9 provided on the top surface, and electrically connecting and fixing the conductive wires 4 with the conductive patterns 9 on the packaging board 10 using an adhesive or the like.

The stacked semiconductor device according to this embodiment comprises a semiconductor chips 1 having top-surface electrodes (first electrodes) 2 on the top surface (first major surface), and back-surface electrodes (second electrodes) 3 or insulation layers 6 on the back surface (second major surface) opposite to the top surface (first major surface), in which a conductive members 4 for connecting the top-surface electrodes 2 with the back-surface electrodes 3 or insulation layers 6 are formed along the outer circumstance of the sides of the semiconductor chips 1, and a packaging board 10 for mounting this semiconductor chips 1. The semiconductor chips 1 are placed on the packaging board 10 at a predetermined angle such as a right angle to the packaging board 10, and the conductive members 4 of the semiconductor chips 1 are connected to the packaging board 10.

In other words, in a semiconductor device comprising semiconductor chips 1 each having electrodes 2 and 3 on the top and back surfaces, respectively, in which the top-surface electrodes 2 are loop-connected with the back-surface electrodes 3 by wire bonding, wires 4 extended

to at least a side of the chips 1 (i.e., top-back connecting terminal or connecting material) are connected to the packaging board 10.

By this, semiconductor chips 1 can be placed at a predetermined angle, such as a right angle, against the packaging board 10, and high-density packaging can be performed.

Eighth Embodiment

Fig. 15 is a sectional view showing a structure of a semiconductor device according to an Eighth Embodiment. A unit comprising a semiconductor chip 1, surface electrodes 2, insulation layer 6, and clip 5 is named as a semiconductor device unit in this embodiment.

An element of the semiconductor device of this embodiment is the semiconductor device unit described referring to Fig. 3, in which conductive clips 5 clamping the top-surface electrodes 2 and the insulation layers 6 on the back surface are provided on one end of each of the semiconductor chips 1. Each of the semiconductor chips 1 has a conductive pattern 9 on the top surface, and are placed on a packaging board 10 perpendicularly to the packaging board 10, and the conductive clips 5 are electrically connected and fixed to the conductive patterns 9 on the packaging board 10.

In the semiconductor device according to this embodiment, semiconductor chips 1 have electrodes 2 and 3 on the top and back surfaces, respectively. These top-surface electrodes 2 and back-surface electrodes 3 are clamped by conductive clips 5, and the conductive clips 5 are extended to at least a side of the chips 1 (i.e., top-back connecting terminal or connecting material) are connected and fixed to the packaging board 10.

Alternatively, in the semiconductor device, the semiconductor chips 7 have top-surface electrodes 2 and insulation layers on the back surfaces which are clamped by conductive clips 5. he conductive clips 5 are extended to at least a side of the chips 1 (i.e., top-back

connecting terminal or connecting material) are connected and fixed to the packaging board 10.

By this, semiconductor chips 1 can be placed at a predetermined angle, such as a right angle, against the packaging board 10, and high-density packaging can be performed.

Ninth Embodiment

Fig. 16 is a sectional view showing a structure of a semiconductor device according to a Ninth Embodiment. A unit comprising a semiconductor chip 1, surface electrodes 2, insulation layer 6 and conductive material 8 is named as a semiconductor device unit in this embodiment.

An element of the semiconductor device of this embodiment is the semiconductor device unit described referring to Fig. 5, in which conductive materials 8 formed over top-surface electrodes 2 and insulation layers 6 on the back surfaces are provided on one side of each of the semiconductor chips 7. The semiconductor chips 7 are placed on a packaging board 10 perpendicularly to the packaging board 10 having conductive patterns 9 on the top surface, and the conductive materials 8 are electrically connected to the conductive patterns 9 on the packaging board 10 using connecting members 9.

In the semiconductor device according to this embodiment, semiconductor chips 1 have electrodes 2 and 3 formed on the top and back surfaces, respectively, these top-surface electrodes 2 and back-surface electrodes 3 are connected by injection-molded conductive materials 8, and the conductive materials 8 formed on at least a side of the chips 1 (i.e., top-back connecting terminal or connecting material) are connected to the packaging board 10.

Alternatively, in the semiconductor device, the back surface of semiconductor chips 1 is insulation-treated, and top-surface electrodes 2 and insulation layers 6 on the back surfaces are connected

by injection-molded conductive materials 8, and the conductive materials 8 formed on at least a side of the chips 1 (i.e., top-back connecting terminal or connecting material) are connected to the packaging board 10.

By this, semiconductor chips can be placed at a predetermined angle, such as a right angle, against the packaging board, and high-density packaging can be performed.

Tenth Embodiment

Figs. 17 and 18 are sectional views showing the structure of a semiconductor device according to a Tenth Embodiment.

In Figs. 17 and 18, reference numeral 11 indicates conductive patterns, and 12 indicates insulators (spacers) on which the conductive patterns 11 are formed.

The semiconductor device of this embodiment is constituted by alternately stacking at least two semiconductor chips 7 having top-surface electrodes 2 and insulation layers 6 formed on the back surface by insulation treatment, and at least two inverted-L-shaped insulators (spacers) 12 having conductive patterns 11 on the circumference thereof as Fig. 18 shows, and electrically connecting the conductive patterns 11 to the top-surface electrodes 2 on the semiconductor chips 7.

In the semiconductor device of this embodiment, a plurality of semiconductor chips 1 having electrodes 2 formed on the major surfaces, and a plurality of insulators (spacers) 12 having conductive patterns 11 on the top surfaces are alternately stacked so that the electrodes 2 of the semiconductor chips 1 are electrically connected with the conductive patterns 11 of the insulators (spacers) 12, and the conductive patterns 11 of the insulators (spacers) 12 adjacent to each other are placed so as to be electrically connected to each other.

The insulators (spacers) 12 have cavities for accommodating the end portions of the semiconductor chips 1, and are stacked so that the conductive patterns 11 of the insulators (spacers) 12 adjacent to each other are placed so as to be electrically connected to each other.

In other words, the connection between electrodes of at least two stacked semiconductor chips is achieved by inserting insulators 12 having conductive patterns (conductive wires) between the chips.

According to this embodiment, the upper and lower semiconductor chips can be electrically connected by stacking the semiconductor chips of the same size, and a stacked semiconductor device can be produced.

Eleventh Embodiment

Figs. 19 and 20 are sectional views showing a structure of a semiconductor device according to an Eleventh Embodiment.

In Figs. 19 and 20, reference numeral 11' indicates other conductive patterns, 12' indicates other insulators (spacers) on which the conductive patterns 11' are formed, 13 indicates still other conductive patterns, 14 indicates boards on which the conductive patterns 13 are formed.

The semiconductor device of this embodiment is constituted by alternately imposing at least two semiconductor chips 7 having top-surface electrodes 2 and insulation layers 6 formed on the back surface by insulation treatment, and at least two insulators 12' having conductive patterns 11' formed on the circumference thereof, as Fig. 20 shows. The top-surface electrodes 2 are connected with the conductive patterns 11'. Supporting board 14 having conductive patterns 13 are provided on the both side of the stacked structure. The conductive patterns 11' on the insulators 12' are connected with with conductive patterns 13 on the substrates 14.

In the semiconductor device of this embodiment, a plurality of semiconductor chips 7 having electrodes 2 on the major surfaces, and

a plurality of insulators (spacers) 12' having conductive patterns 11' on the top surfaces are alternately stacked so that the electrodes 2 of the semiconductor chips 7 are electrically connected with the conductive patterns 11' of the insulators 12', and supporting boards 14 having the conductive patterns 13 are placed so that the conductive patterns 13 of the substrate 14 make contact with the conductive patterns 11' of the insulators 12'.

In other words, the connection between electrodes of at least two stacked semiconductor chips 7 is achieved by connecting conductive patterns 11' of insulators 12' inserted between the chips with conductive patterns 13 on the supporting boards 14 provided on the both sides of the chips 7.

According to this embodiment, the upper and lower semiconductor chips can be electrically connected by stacking the semiconductor chips of the same size, and a stacked semiconductor device can be produced.

The features and the advantages of the present invention as exemplified above may be summarized as follows.

According to one aspect of the present invention, there is provided a semiconductor device comprising a semiconductor chip having electrodes formed on the top surface, and electrodes or an insulation layer on the back surface, in which the top-surface electrodes are loop-connected with the back-surface electrodes or insulation layer by wire bonding. Alternatively, there is provided a semiconductor device of which the top-surface electrodes are connected with the back-surface electrodes or insulation layer by conductive clips, or by deposited conductive materials. By this, even semiconductor chips or semiconductor device units of the same size can be stacked, and a densely packaged semiconductor device can be produced.

According to another aspect of the present invention, there is provided a densely packaged stacked semiconductor device by stacking

semiconductor device units as stated above, and performing mutual electrical connection.

According to another aspect of the present invention, there is provided a densely packaged stacked semiconductor device by mounting a plurality of semiconductor device units as stated above on a packaging board perpendicularly to the packaging board.

According to still another aspect of the present invention, there is provided a densely packaged stacked semiconductor device by stacking a plurality of semiconductor chips and spacers having conductive wires on the surface, and establishing mutual connection between electrodes.

Obviously many modifications and variations of the present invention are possible in the light of the above teachings. It is therefore to be understood that within the scope of the appended claims the invention may by practiced otherwise than as specifically described.

The entire disclosure of a Japanese Patent Application No. 2000-33790, filed on February 10, 2000 including specification, claims, drawings and summary, on which the Convention priority of the present application is based, are incorporated herein by reference in its entirety.

CLAIMS

1. A semiconductor device comprising:

a semiconductor chip;

at least a first electrode formed on the first major surface of said semiconductor chip,

at least a second electrode or an insulation layer formed on the second major surface opposite to said first major surface; and

at least a conductive member for connecting said first electrode with said second electrode or said insulation layer, said conductive member being formed along the outer circumference of at least a side of said semiconductor chip.

2. The semiconductor device according to claim 1, wherein each of said conductive members is comprised of a wire bonded to said first electrode and said second electrode.

3. The semiconductor device according to claim 1, wherein each of said conductive members is comprised of a conductive clip holding said first electrode together with said second electrode or said insulation layer.

4. The semiconductor device according to claim 1, wherein each of said conductive member is comprised of conductive layer formed on the surface of said semiconductor chip extending from said first electrode to said second electrode or said insulation layer.

5. A semiconductor device comprising:

a plurality of semiconductor device units, each of said semiconductor device units including:

a semiconductor chip;

at least a first electrode formed on the first major surface of said semiconductor chip,

at least a second electrode or an insulation layer formed on the second major surface opposite to said first major surface; and

at least a conductive member for connecting said first electrode with said second electrode or said insulation layer, said conductive member being formed along the outer circumference of at least a side of said semiconductor chip;

wherein said semiconductor device units are stacked each other, and said conductive members are connected to each other.

6. The semiconductor device according to claim 2, wherein a first chip has a first conducting pattern extended from said first electrode, a second chip has a second conducting pattern extended from said second electrodes, and a bump is provided between said first conducting pattern and said second conducting pattern, which face to each other, for electrically connecting said two conducting patterns.

7. The semiconductor device according to claim 5, wherein each of said conductive members is comprised of a wire bonded to said first electrode and said second electrode.

8. The semiconductor device according to claim 5, wherein each of said conductive members is comprised of a conductive clip holding said first electrode together with said second electrode or said insulation layer.

9. The semiconductor device according to claim 5, wherein each of said conductive member is comprised of conductive layer formed on the surface of said semiconductor chip extending from said first electrode to said second electrode or said insulation layer.

10. A semiconductor device comprising:

a plurality of semiconductor device units, each of said semiconductor device units including:

a semiconductor chip;

at least a first electrode formed on the first major surface of said semiconductor chip,

at least a second electrode or an insulation layer formed on the second major surface opposite to said first major surface; and

at least a conductive member for connecting said first electrode with said second electrode or said insulation layer, said conductive member being formed along the outer circumference of at least a side of said semiconductor chip;

a packaging board for mounting said plurality of semiconductor device units;

wherein said semiconductor device units are placed on said packaging board so as to have a predetermined angle to said packaging board, and said conductive members of said semiconductor device units are connected to said packaging board.

11. The semiconductor device according to claim 10, wherein each of said conductive members is comprised of a wire bonded to said first electrode and said second electrode.

12. The semiconductor device according to claim 10, wherein each of said conductive members is comprised of a conductive clip holding said first electrode together with said second electrode or said insulation layer.

13. The semiconductor device according to claim 10, wherein each of said conductive member is comprised of conductive layer formed on

the surface of said semiconductor chip extending from said first electrode to said second electrode or said insulation layer.

14. A semiconductor device comprising:

a plurality of semiconductor chips each having electrodes formed on the major surface thereof, and

a plurality of spacer members each having conductive pattern on the surface thereof;

wherein said semiconductor chips and said spacer members are stacked alternately such that said electrodes of said semiconductor chips are electrically connected to said conductive patterns of said spacer members, and said conductive patterns of said spacer members are electrically connected to each other.

15. The semiconductor device according to claim 14, wherein each of said spacer members has a cavity for accommodating the end portion of said semiconductor chip.

16. The semiconductor device according to claim 14, further comprising supporting members having conductive patterns thereon, wherein said supporting members are placed so as to make said conductive patterns thereof contact with said conductive patterns of said plurality of spacer members.

Abstract of the Disclosure

In a semiconductor chip having electrodes formed on the top surface, and electrodes or an insulation layer formed on the back surface, the top-surface electrodes are loop-connected with the back-surface electrodes by wire bonding, or, the top-surface electrodes are connected with the back-surface electrodes or an insulation layer by conductive clip, or by deposited conductive materials. The semiconductor chips thus produced are stacked, and wires, conductive clips, or conductive materials are connected and fixed to each other to produce a stacked semiconductor device in which semiconductor chips of the same size are densely packaged. Thus, a semiconductor device is provided which enables high-density packaging of semiconductor chips even of the same size.

Fig. 1

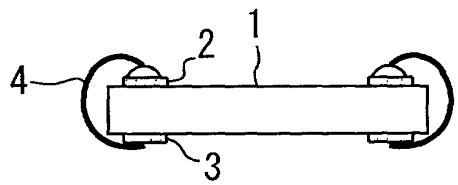


Fig. 2

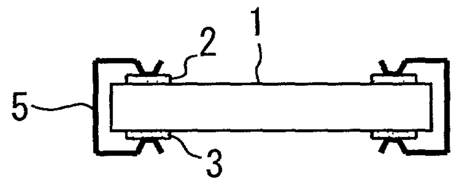


Fig. 3

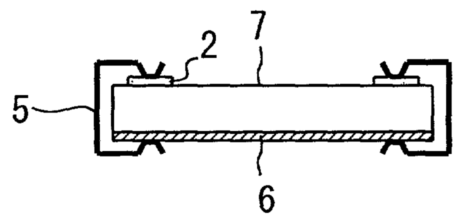


Fig. 4

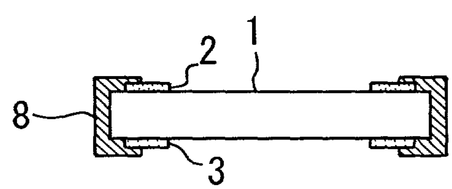


Fig. 5

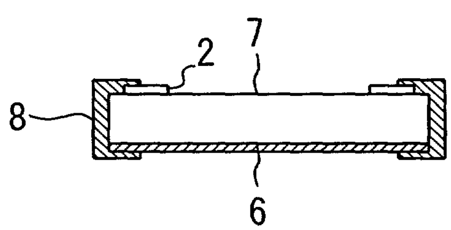


Fig. 6

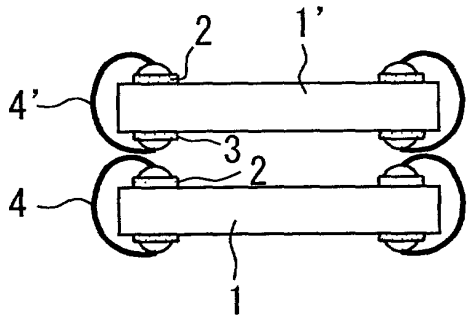


Fig. 7

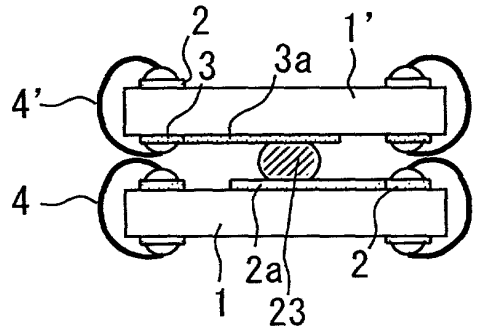


Fig. 8

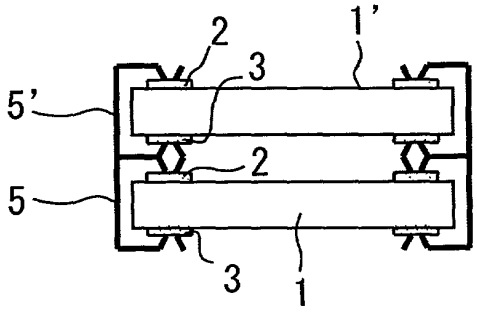
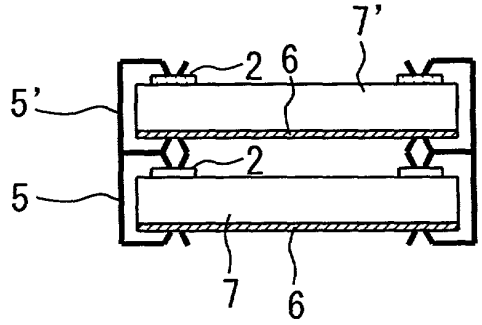


Fig. 9



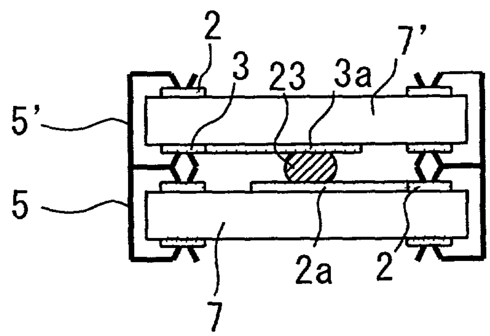


Fig. 10

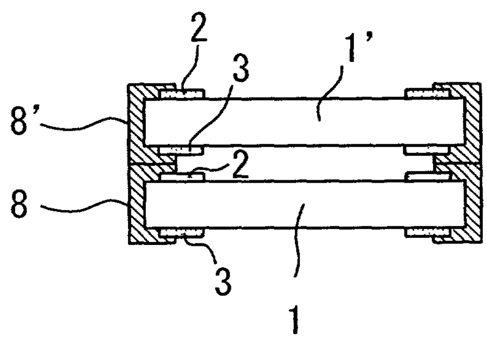


Fig. 11

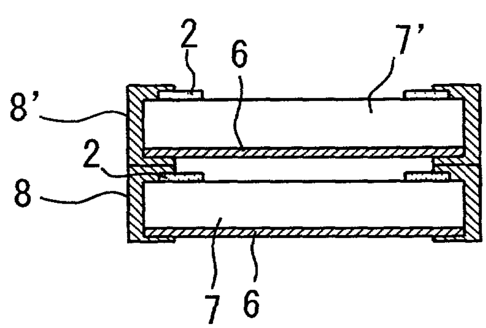


Fig. 12

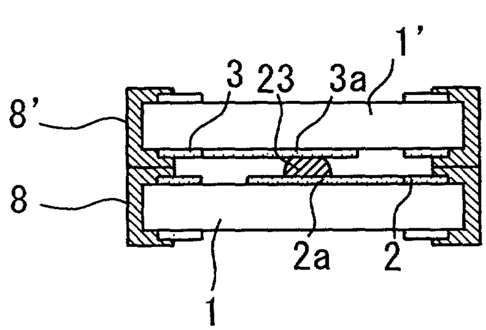


Fig. 13

Fig. 14

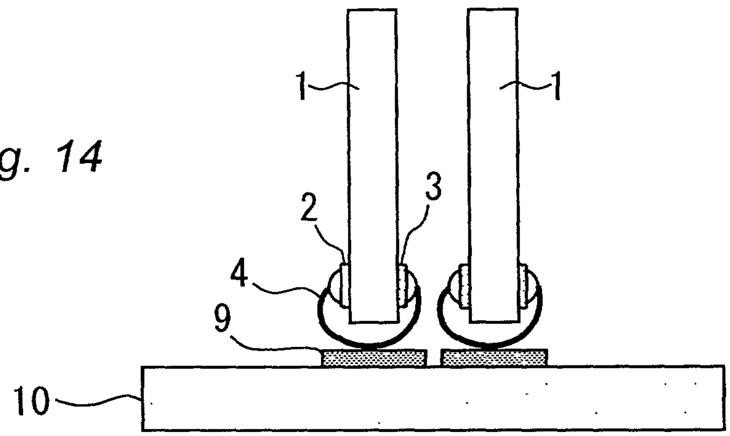


Fig. 15

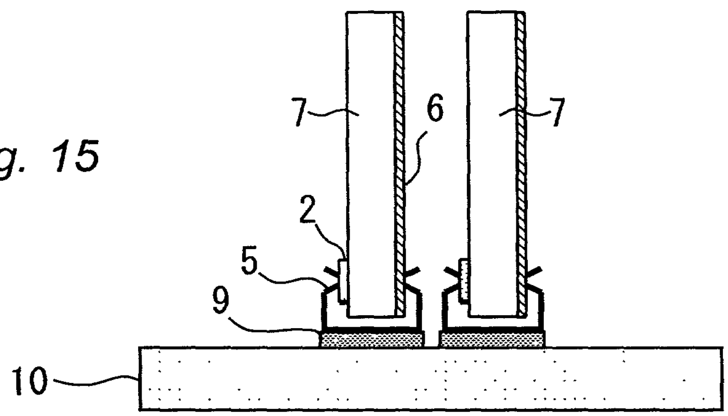


Fig. 16

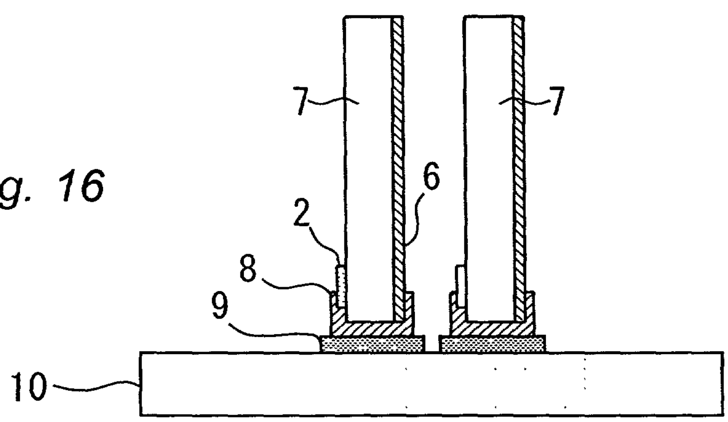


Fig. 17

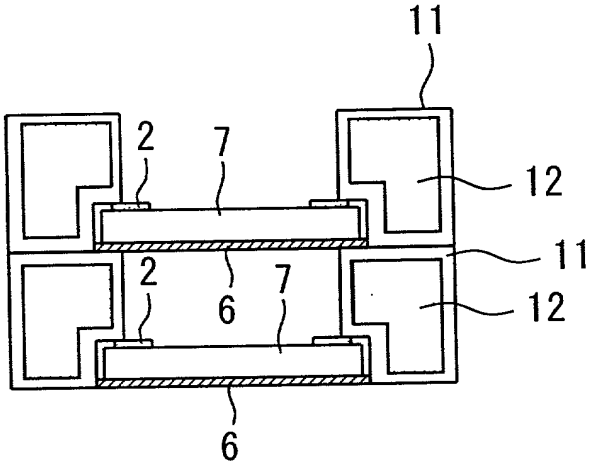


Fig. 18

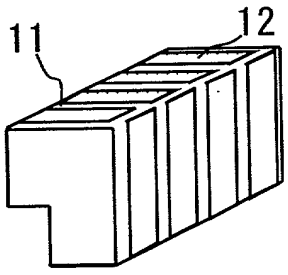


Fig. 19

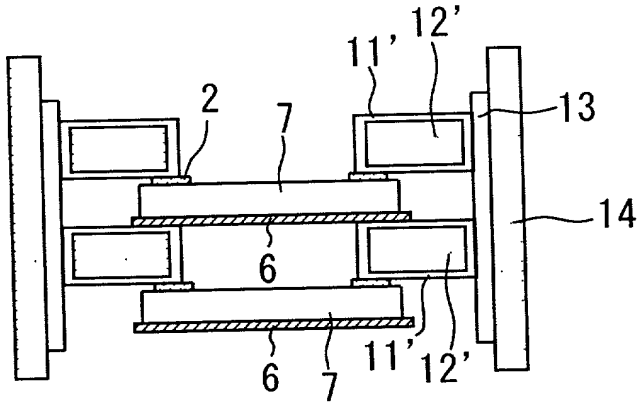


Fig. 20

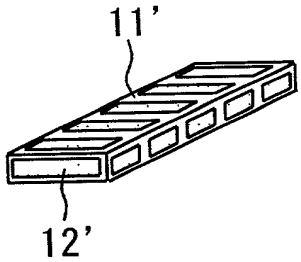
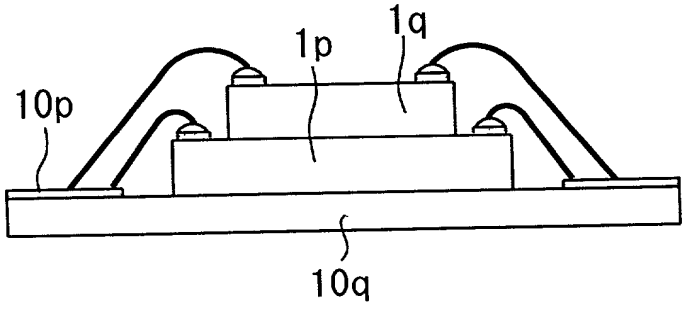


Fig. 21



4264 US
5207434501

Declaration and Power of Attorney For Patent Application
特許出願宣言書及び委任状
Japanese Language Declaration
日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者（下記の名称が複数の場合）であると信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled.

SEMICONDUCTOR DEVICE HAVING DENSELY STACKED SEMICONDUCTOR CHIPS

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ ___月___日に提出され、米国出願番号または特許協定条約国際出願番号を _____とし、
(該当する場合) _____に訂正されました。

☐ was filed on_____
as United States Application Number or
PCT International Application Number
_____ and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第 37 編第 1 条 56 項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第 35 編 119 条(a)-(d)項又は 365 条(b)項に基づき下記の、米国以外の国の少なくとも一ヵ国を指定している特許協力条約 365 (a)項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Not Claimed 優先権主張なし
2000-033790	Japan	10 / February / 2000	☐
			☐

私は、第 35 編米国法典 119 条(e)項に基づいて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United Slates Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第 35 編 120 条に基づいて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約 365 条(c)に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第 35 編 112 条第 1 項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第 37 編 1 条 56 項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自信の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第 18 編第 1001 条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
(日本語宣言書)

委任状：　私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。
(弁護士、または代理人の指名及び登録番号を明記のこと)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: (list name and registration number)

Edward A. Becker, Reg. No. 37,777; Stephen A. Becker, Reg. No. 26,527; John G. Bisbikis, Reg. No. 37,095; Daniel Bucca, Reg. No. 42,368; Kenneth L. Cage, Reg. No. 26,151; Stephen C. Carlson, Reg. No. 39,929; Paul Devinsky, Reg. No. 28,553; Laura A. Donnelly, Reg. No. 38,435; Margaret M.Duncan, Reg. No. 30,879; Brian E. Ferguson, Reg. No. 36,801; Michael F. Fogarty, Reg. No. 36,139; Wilhelm F. Gadiano, Reg. No. 37,136; Keith E. George, Reg. No. 34,111; John A. Hankins, Reg. No. 32,029; Thomas A. Jolly, Reg. No.39,241; Eric J. Kraus, Reg. No. 36,190; Edward E. Kubasiewicz, Reg. No. 30,020; Patrick B. Law, Reg. No. 41,549; Robert E. LeBlanc, Reg. No. 17,219; Jack Q. Lever, Reg. No. 28,149; Raphael V. Lupo, Reg. No. 28,363; Christine F. Martin, Reg. No. 39,762; Michael E. McCabe, Jr., Reg. No. 37,182; James H. Meadows, Reg. No. 33,965; Michael A. Messina, Reg. No. 33,424; Eugene J. Molinelli, Reg. No. 42,901; Joseph H. Paquin, Jr., Reg. No.31,647; Craig L. Plastrik, Reg. No. 41,254; Robert L. Price, Reg. No. 22,685; Paul A. Roberts, Reg. No. 40,289; Gene Z. Rubinson, Reg. No. 33,351; Joy Ann G. Serauskas, Reg. No. 27,952; Michele M. Schafer, Reg. No. 34,717; David J. Serbin, Reg. No. 30,589; Glenn Snyder, Reg. No. 41,428; Arthur J. Steiner, Reg. No. 26,106; David L. Stewart, Reg. No. 37,578; Leonid D. Thenor, Reg. No. 39,397; Keith J. Townsend, Reg. No. 40,358; Leon R. Turkevich, Reg. No. 34,035; Christopher D. Ward, Reg. No. 41,367; Damian G. Wasserbauer, Reg. No. 34,749; Aaron Weisstuch, Reg. No. 41,557; Edward J. Wise, Reg. No. 34,523; Alexander V. Yampolsky, Reg. No. 36,324; and Robert W. Zelnick, Reg. No. 36,976

書類送付先

Send Correspondence to:

McDermott, Will & Emery
600 13th Street, N.W.
Washington, D.C.　20005-3096

直接電話連絡先：(名前及び電話番号)

Direct Telephone Calls to: (name and telephone number)

Stephen A. Becker
(202) 756-8608

単独発明者または第一の共同発明者の氏名	Full name of sole or first joint inventor Kozo HARADA
発明者の署名　日付	Inventor's signature　Date Kozo Harada　July, 31, 2000
住所	Residence Tokyo, JAPAN
国籍	Citizenship Japanese
郵便の宛先	Post Office Address c/o Mitsubishi Denki Kabushiki Kaisha 2-3, Marunouchi 2-chome Chiyoda-ku, Tokyo 100-8310 JAPAN

第二の共同発明者の氏名	Full name of second joint inventor, if any Hiroshi SAWANO
第二の共同発明者の署名　日付	Second joint Inventor's signature　Date Hiroshi Sawano　July, 30, 2000
住所	Residence Tokyo, JAPAN
国籍	Citizenship Japanese
郵便の宛先	Post Office Address c/o Mitsubishi Denki Kabushiki Kaisha 2-3, Marunouchi 2-chome Chiyoda-ku, Tokyo 100-8310 JAPAN

(第三以降の共同発明者についても同様に記載し、署名すること)

(Supply similar information and signature for third and subsequent joint inventors.)